ABSTRACT

Hardware Implementation of Speech Compression Algorithms
For Voice over Internet Telephony

Marcus Lloyde George

Voice-over Internet Protocol (VoIP) telephony which is the transmission of real-time voice over an internet protocol (IP) data network, is increasingly becoming a variant telecommunication technology that one day may surpass the old analog and digital telephone systems. The Quality-of-Service (QoS) factor is an important parameter to be considered when measuring the performance of a VoIP system. Algorithmic delay (latency) may influence the QoS of a VoIP system.

This thesis presents the hardware implementation of the Pulse Code Modulation (PCM), Adaptive-Differential Pulse Code Modulation (ADPCM) and Conjugate-Structure Algebraic-Code-Excited Linear-Prediction (CS-ACELP) speech compression algorithms. The speech compression algorithms were implemented in hardware using Xilinx 11.1 ISE, after which ITU-T test vectors were used to determine whether they were equivalent implementations of the speech compression algorithms. The algorithmic delays of hardware-implemented speech compression algorithms were obtained via simulation using Modelsim XE 6.4b while the algorithmic delays of the software-implemented speech compression algorithms were obtained by software profiling using the GPROF profiler.

After comparison the algorithmic delays of the hardware-implemented speech compression algorithms were found to be shorter than the algorithmic delays of their software-implemented counterparts. The latency of these hardware implemented speech compression algorithms were them compared with that of existing hardware implementations.

Keywords: Marcus Lloyde George; Hardware Implementation; Speech Compression Algorithm; Speech Processing.