ABSTRACT

Wavelet Synthesis Cores for Image Data Compression and Decompression

Ricardo Orlando Paharsingh

Recent developments in Programmable Asics (Application-Specific Integrated Circuits) such as Field Programmable Gate Arrays (FPGAs) and other Complex programmable Logic Devices (CPLDs) [1] have opened new avenues in designing digital systems and particularly a new area of investigation called "Hardware Compilation". Different algorithms in signal processing, computer architecture, digital communications, soft computing, etc, can be implemented in hardware using these devices with significant advantages in terms of reconfiguration, processing time and integration as system-on-a-chip. This research will investigate and implement the section of digital communications and signal processing concerned with transforming images for compression. The advantages pointed out above will be integrated in the design process to develop cost effective hardware modules.

Image transmission and storage have increased significantly in just a few years. To reduce the bandwidth required a large amount of research is aimed at developing better image compression schemes, particularly transform algorithms which is the first stage in image compression. Transform algorithms such as the cosine transform and the wavelet transform are the source of power behind schemes such as JPEG (Joint Photographic Experts Group) and JPEG2000 [2], which is the image compression format that offers highest compression. The transform algorithms are a mathematical means for de-correlating a signal such as an image in an effort to increase the probabilities chosen symbols (data sets) within the signal. The data sets are then fed through an optional quantizer to further increase the probabilities (with the loss of data) and then to an

entropy encoder which will use the probabilities to achieve compression. Today, the wavelet transform [1, 4 – 6, 10, 12 – 13, 19 – 24, 29 – 33] has become a well-established and the most powerful tool for transforming images. This is because it offers a multi-resolution analysis of the signal in both the time and frequency domain resulting in a more efficient de-correlation of the signal and increased probabilities of the chosen symbols. In this research efficient and fast wavelet cores for image data compression and decompression was verified through simulations and implemented as hardware for stand-alone applications or library usage on low cost FPGA chips. Specific filters which are a part of the JPEG2000 standard part 2 were used. These filters were chosen for speed, the efficient use of hardware resources and their ability to de-correlate images. Fast filters were chosen based on the number of computations required, the lack of floating computations and where multiplication, division can be implemented in terms of shifting. By eliminating these computational units it unavoidable results in a minimum amount of hardware resources since no hardware is required for their implementation. The ability to de-correlate was determined by experimental comparisons [5] of a large number of filters. The final product is available for use as part of any hardware image compression system which implements the JPEG2000 standard.

Keywords: Ricardo Orlando Paharsingh; Image Data Compression; Wavelet Transform; JPEG2000; Hardware Compilation; FPGA