ABSTRACT

ANALYSIS, DESIGN AND FPGA IMPLEMENTATION OF AN NCO

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The Numerically Controlled Oscillator (NCO) designed in this project, is for the ASIC implementation of the down/up conversion of 15 MHz carriers in the Rx/Tx paths respectively of a UMTS/CDMA Base Station platform, being developed at Lucent Technologies. This work presents a low cost and optimal implementation of an NCO that provides 1kHz frequency resolution and a minimum Spurious Free Dynamic Range (SFDR) of 75 dBc at sample frequencies of 76.8 MHz and 153.6 MHz.

The project focuses on an in- depth analysis of various implementations of the NCO in order to achieve the required specifications. Existing schemes of NCO components are used in the analysis, but the final design and VHDL implementation of these components, as well as that of the overall NCO is a novelty.

This document will show that this analysis was done with simulations and comparisons of those in MATLAB®. The VHDL implementation of the chosen design is then discussed, and the results of these simulations in Model Tech's ModelSim® are compared with those obtained in MATLAB®. The design's functionality is finally tested on an XESS FPGA development board using a Xilinx® Spartan2™ 100, 000–gate FPGA and the Xilinx® ISE 4.1i design environment to ensure that design specifications were met.