ABSTRACT

Novel Multi-Precision Floating-Point Multiplier Architecture

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Arithmetic Logic Units (ALUs) are very important components of processors performing arithmetic operations such as multiplication, division, addition, subtraction, cubing and squaring. Of all operations, multiplication is most frequently used in ALUs. Floating-point multiplication is a very important component of many engineering applications such as signal processing, video processing and image processing. The dynamic range of numbers represented by floating-point arithmetic is very large when compared to fixed-point numbers of the same bit-width. This thesis presents the development of a novel multi-precision floating-point multiplier architecture that can be used in data intensive applications, requiring variable precision and low path delay. The Novel Multi-Precision Floating-Point Multiplier Architecture can be configured to operate in single, double, quadruple and octuple precision modes as set out by IEEE-754 standards for floating-point numbers. The system is also prepared for increased throughput and utilizes a novel technique called mantissa similarity investigation in further reducing the path delay of the system. The system was synthesized for a variety of FPGA targets using Xilinx ISE Design Suite 14.7 Commercial Edition and performance was simulated with ISIM and other tools available from Xilinx ISE Design Suite 14.7. The implemented system was thereafter compared with existing implementations of floating-point multipliers at various precision levels in terms of path delay, throughput and precision range for computations performed. After comparison, it was concluded that the novel multi-precision floating-point multiplier architecture had shorter path delay, provided multiplication for a wider dynamic range of numbers and performed floating point multiplication on larger number of batches of inputs per unit time, than existing multiplier architectures.

Keywords: Arithmetic Circuits; Floating-Point Multiplier; Multi-Precision Floating Point; Arithmetic Logic; FPGAs in Arithmetic.